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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,823	02/20/2004	Yoshikatsu Tanaka	WAKA 20.997(100957-00084	7053

26304 7590 01/12/2006

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EXAMINER	
KINKEAD, ARNOLD M	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,823	TANAKA, YOSHIKATSU	
	Examiner	Art Unit	
	Arnold M. Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Pollard(US 4,627,533 new cite).

The reference by Pollard discloses a temperature compensated crystal oscillator, the oscillator circuit is shown in figures 2 and 3. The package is hermetically sealed(see figure 2, and col.4, lines 24-30; In figure 2, the elements/circuit components(resonator crystal 72, a circuit component) is shown mounted on the surface of the substrate(42) in a cavity(44). Figure 3 shows the substrate circuit pattern and shows mounting electrodes(64,66,74,76) on the reverse side. Cols. 1-col. 2 describe the use of temperature compensation circuit(68,70) outside of the crystal cavity that allows for to directly compensating the crystal oscillator. Note chip mounted compensation circuit (70), see col. 3, lines 35-end.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims, 4,5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollard(' 533) in view of Kimura et al (US 6,487,085 cited previously) .

The reference by Pollard discloses a temperature compensated crystal oscillator, the oscillator circuit is shown in figures 2 and 3. The package is hermetically sealed(see figure 2, and col.4, lines 24-30; In figure 2, the elements/circuit components(resonator crystal 72, a circuit component) is shown mounted on the surface of the substrate(42) in a cavity(44). Figure 3 shows the substrate circuit pattern and shows mounting electrodes(64,66,74,76) on the reverse side. Cols. 1-col. 2 describe the use of temperature compensation circuit(68,70) outside of the crystal cavity that allows for to directly compensating the crystal oscillator. Note chip mounted compensation circuit (70), see col. 3, lines 35-end.

The reference by Pollard does not show conventional dimensions in (mm) for the chip components. With regard to the latter, the reference by Kimura et al discloses the same dimensions, i.e. 0.6mmX 0.3mm as the size of the chip capacitors(23a, fig.1), see col.5, lines 38-42. These dimensions allow for other elements to share cavity space, for example. Also, an adjustable varactor element for adjusting frequency via an external line is not shown. With

regards this capacitor, Kimura, also shows such an element, see figure 2, element 32, that will allow for frequency adjustment via terminal 34e.

In light of the above it would have been obvious to one of ordinary skill in the art, at the time of the invention, to have recognized the importance of having the proper size dimensions, as noted above by Kimura et al, to allow for the chip elements and crystal to be recessed together. The specific dimension being dependent on the overall desired package size and Kimura et al serves to highlight the use of 0.6mmX0.3mm dimension. The overall function of the elements do not change and thus the reference by Jiles et al could have used such dimensioned chip elements to allow for a particular package size. The use of a varactor is also conventional as highlighted in Kimura, for allowing further frequency control as desired with temperature compensation as well to move towards the desired frequency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M. Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead

Jan. 05, 2006